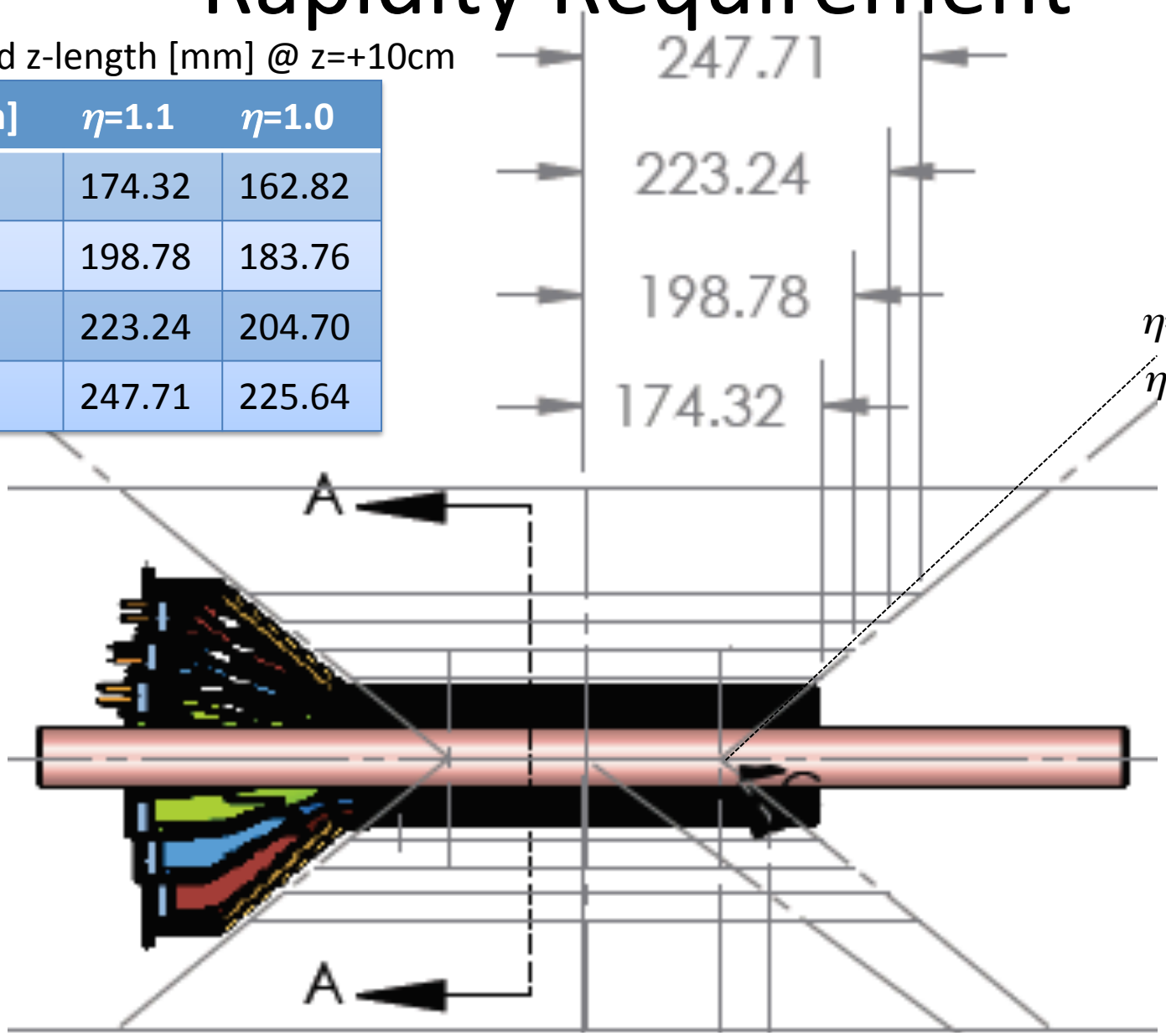
Longer INTT Design

RIKEN/RBRC
Itaru Nakagawa

Rapidity Requirement

Required z-length [mm] @ z=+10cm

r [cm]	η=1.1	η=1.0
6	174.32	162.82
8	198.78	183.76
10	223.24	204.70
12	247.71	225.64



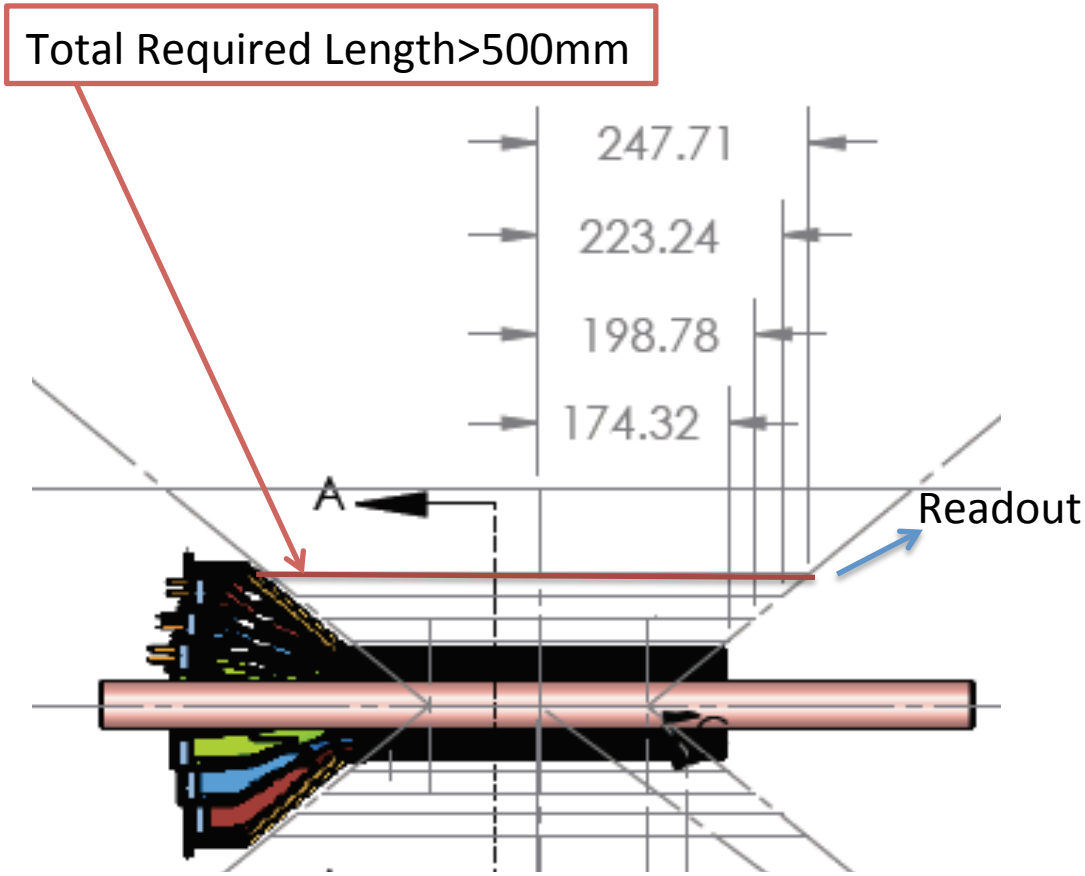
Constraints

- Total number of ROC input channels (# of chips limitation)
- Don’t want to have customized design for all 4 layers. Introduces too many complications and difficulties and costs.
- Maximum Silicon sensor length is 135mm for 22.5mm width (comes from 6 inch wafer).
- Technical limit of the HDI size (width, length).

Single Side Readout

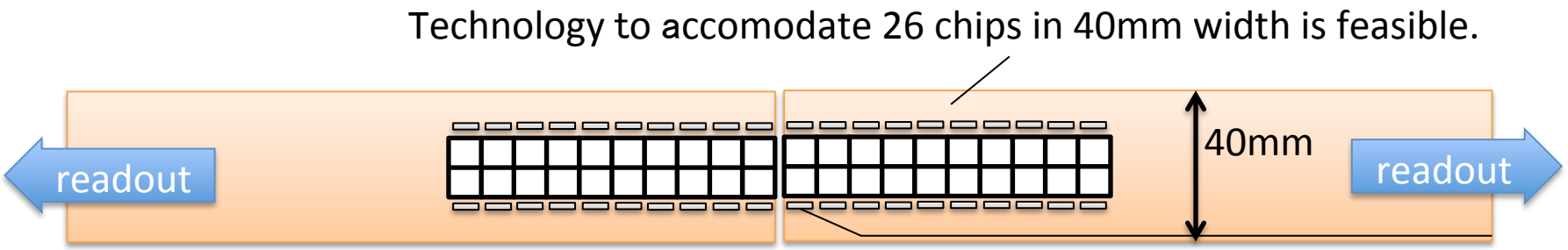
Due to the occupied space by MAPS readout in one side, INTT doesn't have space to readout from the same side of MAPS.

If we have to readout from one side, the signal needs to be transfer all the way from the one end to the other. The length will be at least 500mm. This is a major technical challenge. The present HDI company never have experience.

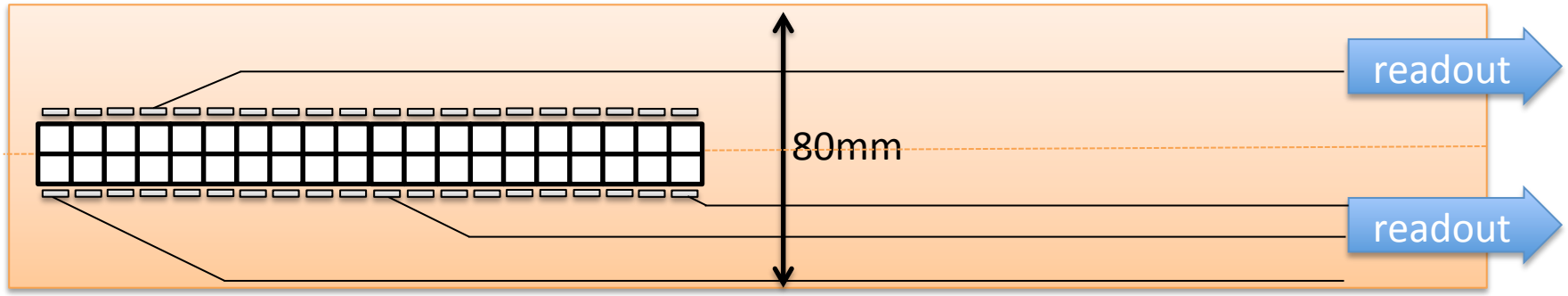


Price we pay for Single Side Readout

- Double Side Readout Design (Present)

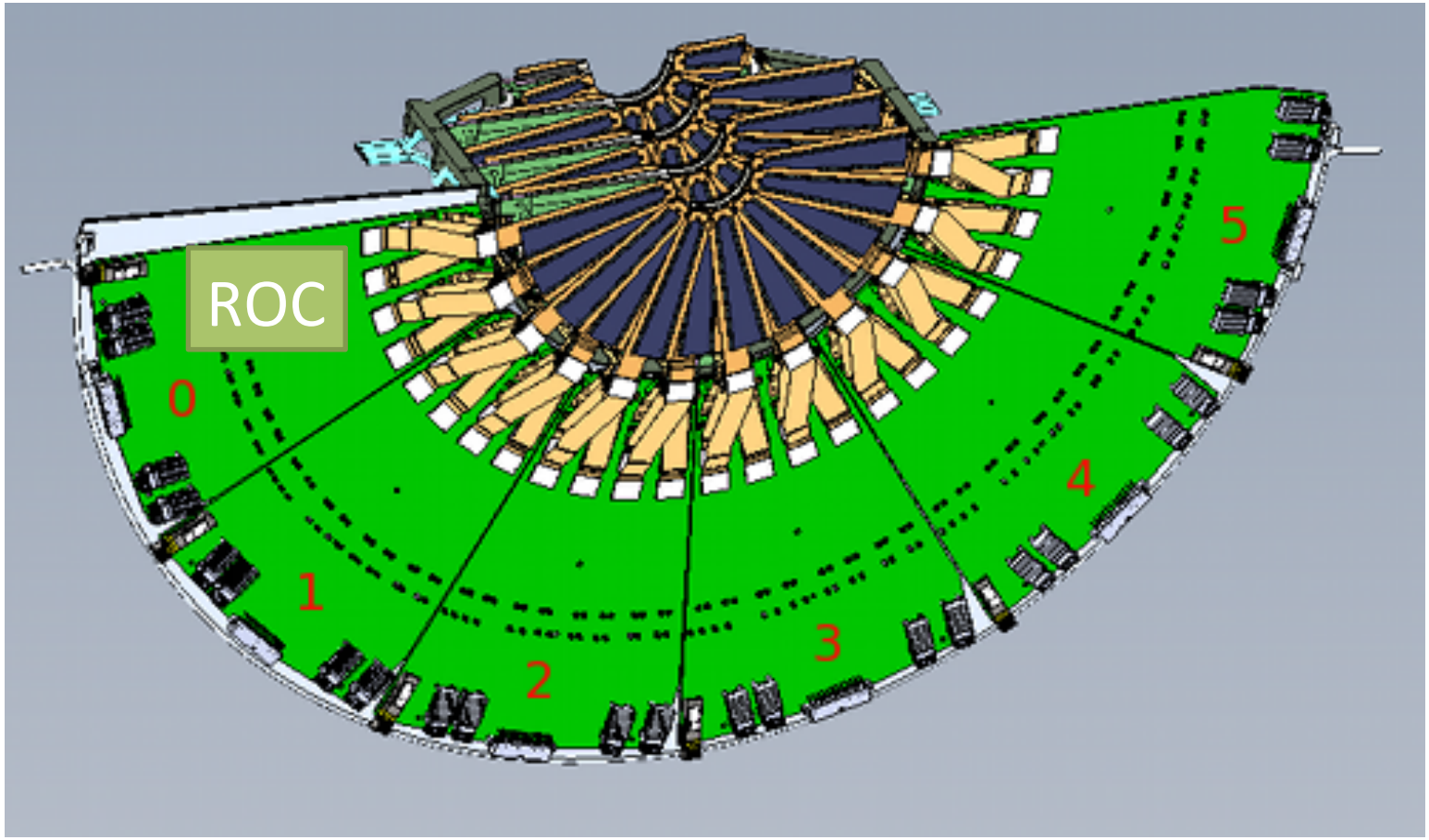


- Single Side Readout Design

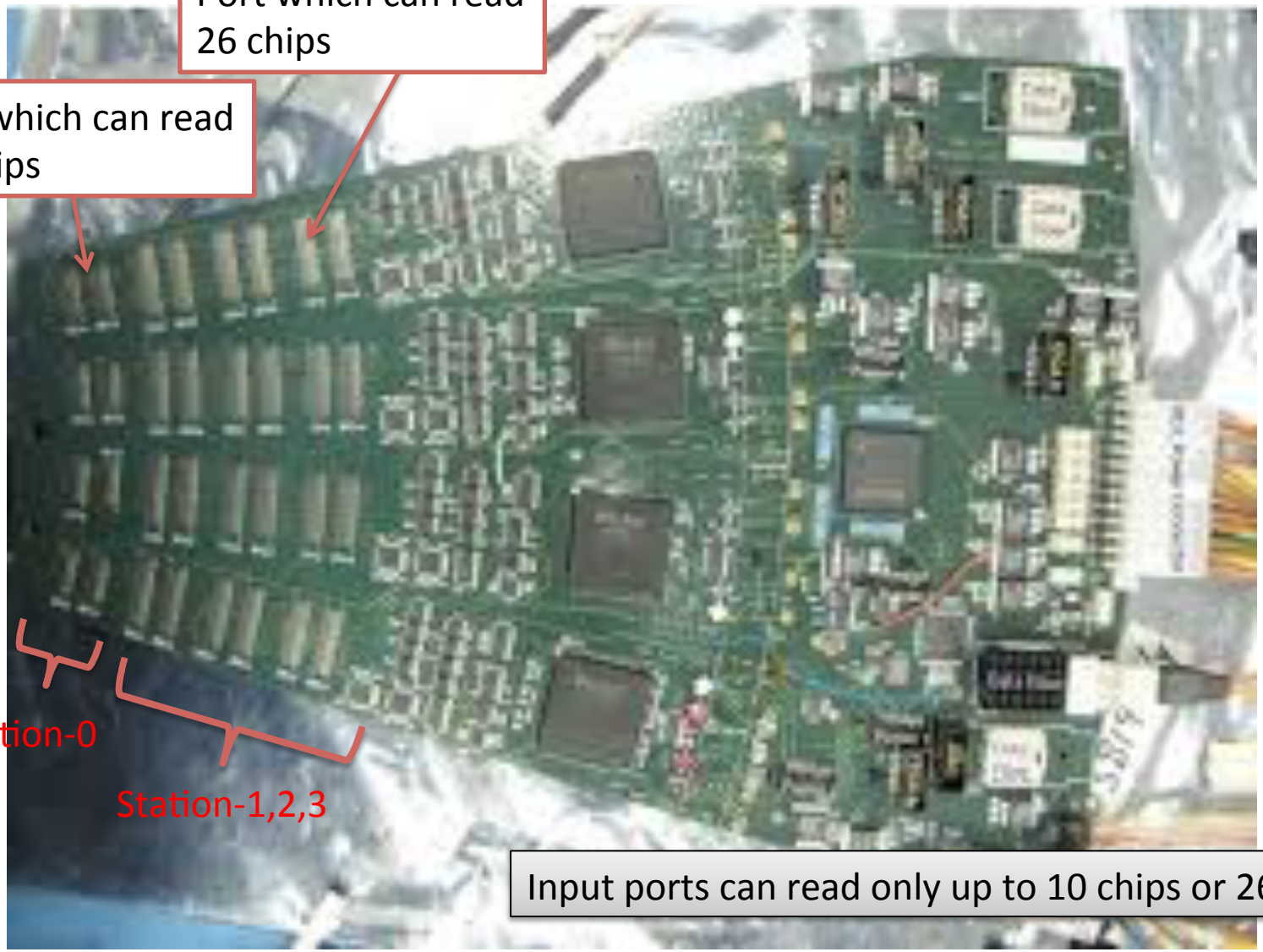


We know the HDI width is at least 40mm in order to fit all the circuit to readout 26 chips. If we double the number of chips to readout, then the HDI width will be also doubled. This will ends up with doubling the radiation length of INTT. **We don't think this is the direction we want to go as a consensus of sPHENIX tracker team.**

Constraints from FVTX



FVTX Input ports of ROC



Input ports can read only up to 10 chips or 26 chips.

ROC Total Number of Ports/Arm

	Per Arm	Total (2 arms)
Station-0	48	96
Station-1,2,3	144	288

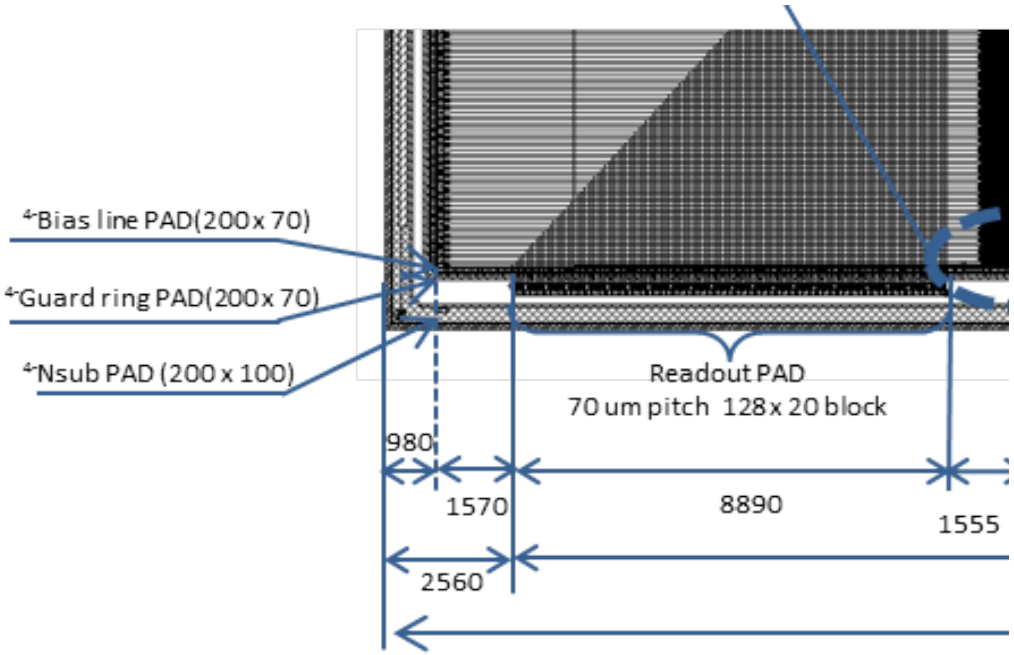
Number of Ladders for sPHENIX INTT

R [cm]	Per Arm	Total (2 arms)
6 (Layer 0)	18	36
8 (Layer 1)	24	48
10 (Layer 2)	30	60
12 (Layer 3)	36	72
Total	**108**	**216**

Basically, all INTT readouts can be fit within Station-1,2,3 ports of the ROC.

Silicon Sensors

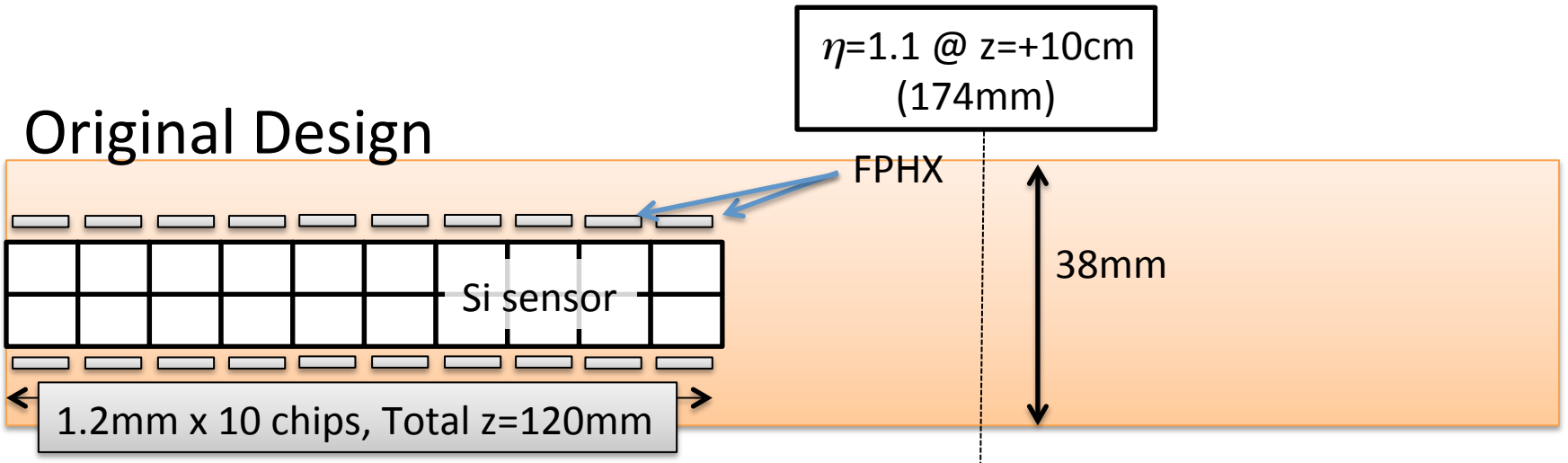
- No ganging.



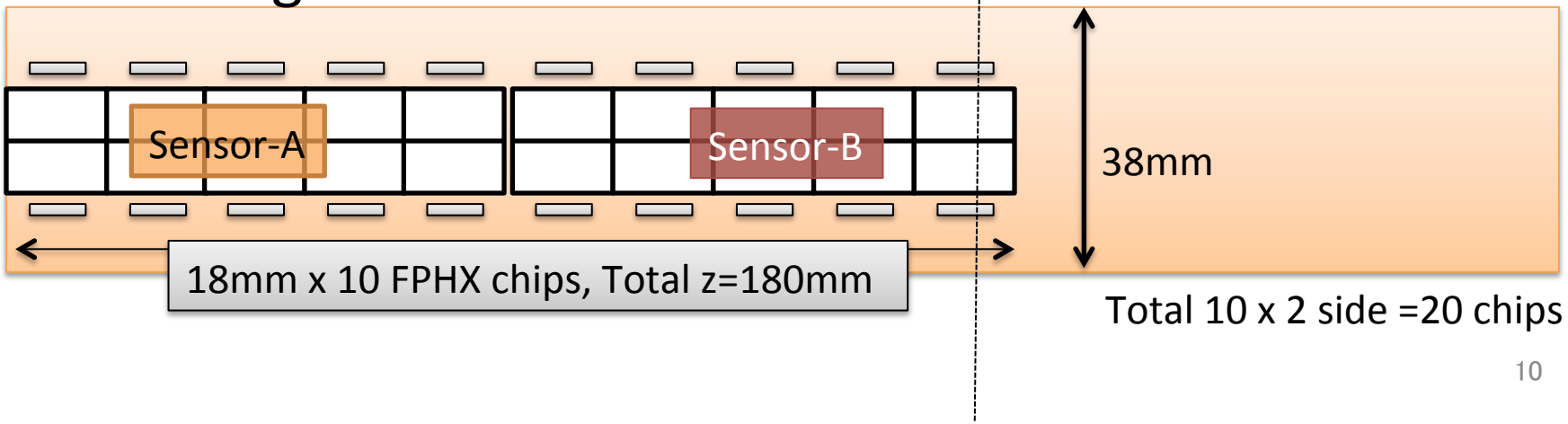
Silicon Sensor
78μm pitch
128 channel/cell
Total width=10mm + α

Original and Layer-0 New Design

- Original Design

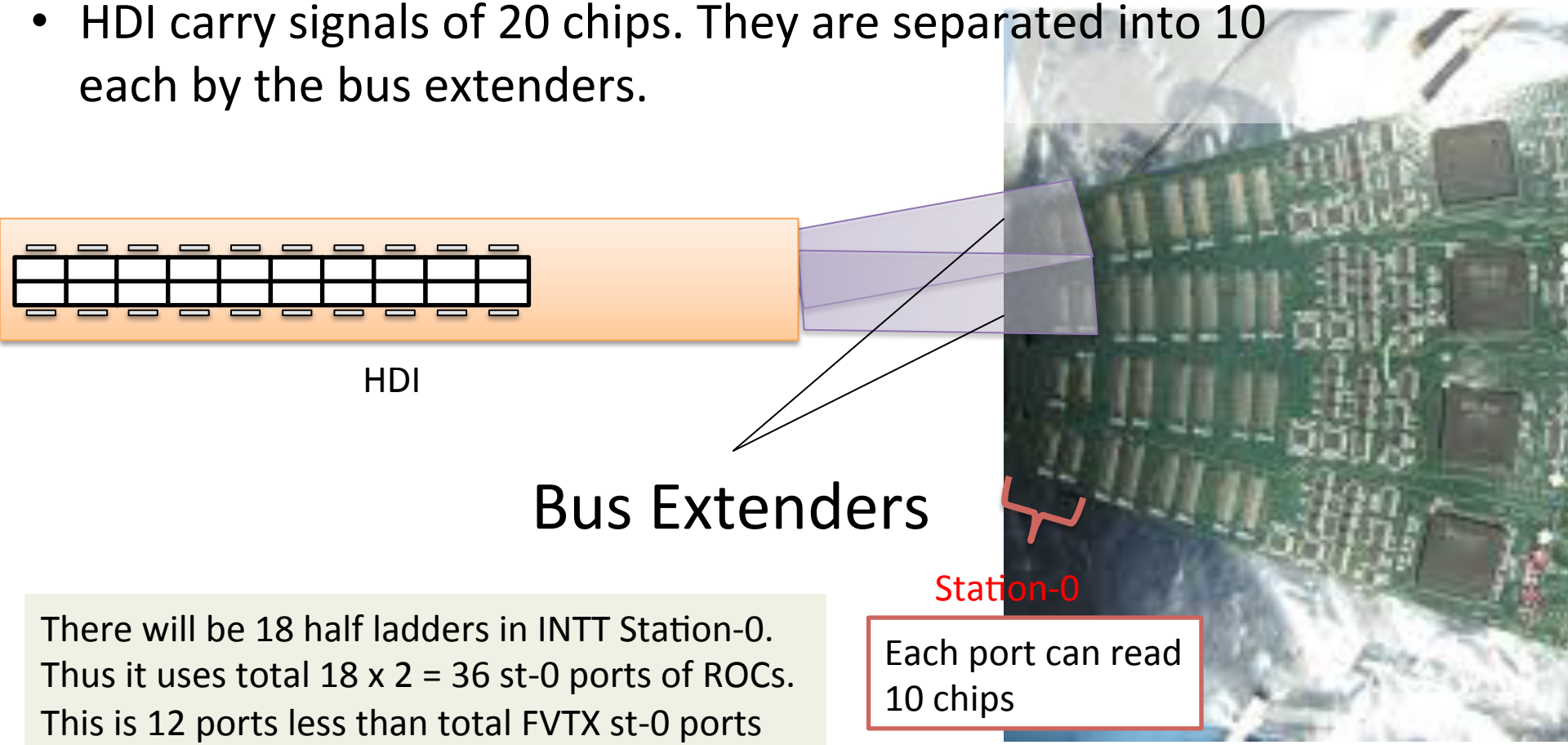


- New Design



ROC Port Allocation for Layer-0

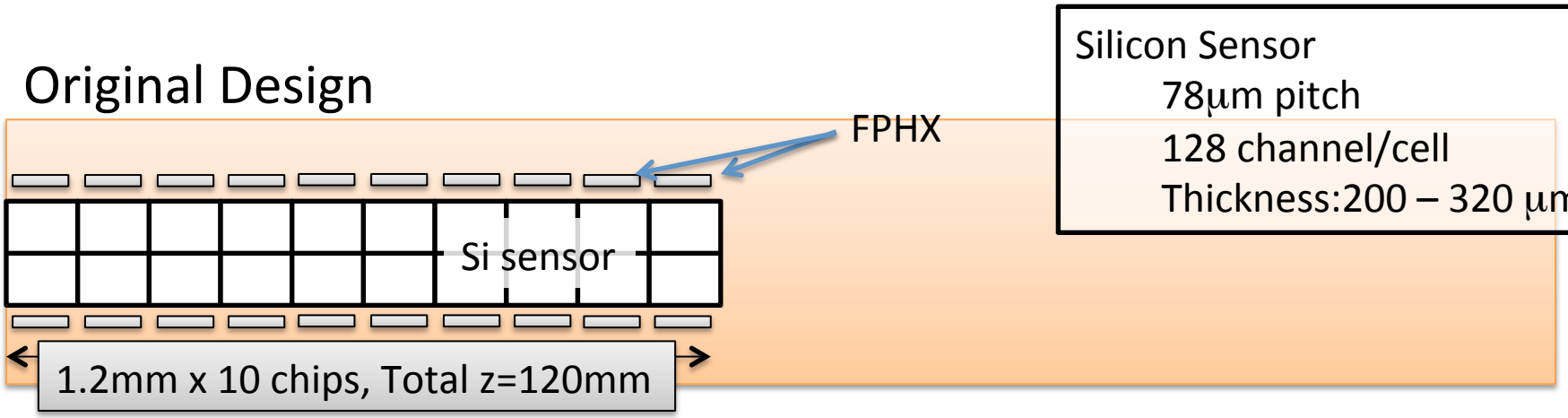
- Layer-0 signals are connected to Station-0 ports of FVTX.
- HDI carry signals of 20 chips. They are separated into 10 each by the bus extenders.



There will be 18 half ladders in INTT Station-0. Thus it uses total 18 x 2 = 36 st-0 ports of ROCs. This is 12 ports less than total FVTX st-0 ports (48 ports)

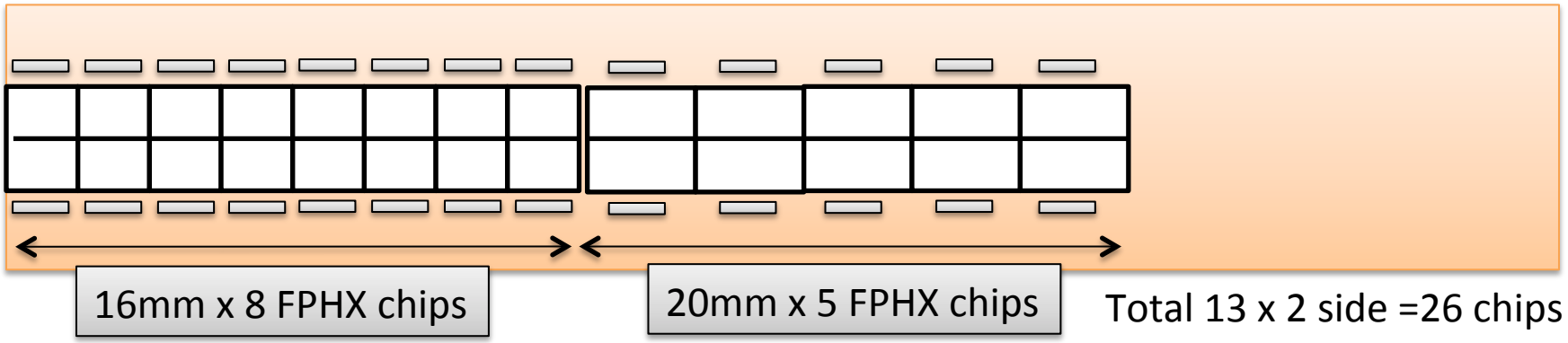
Original and Layer-1,2,3 New Design

- Original Design



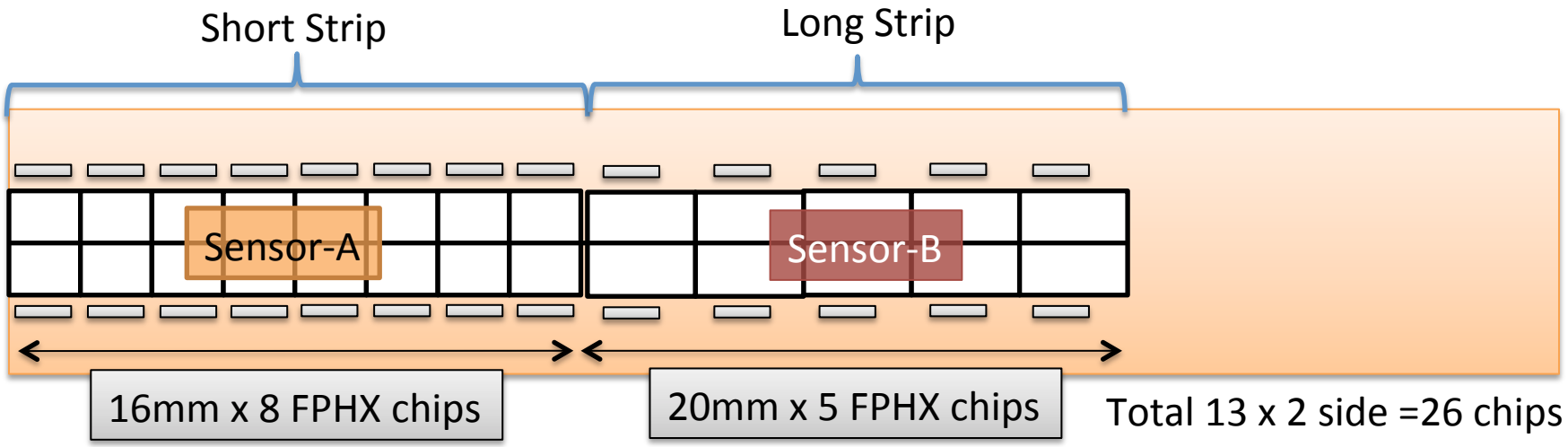
Silicon Sensor
78μm pitch
128 channel/cell
Thickness:200 – 320 μm

- New Design



Layer-1,2,3 New Design Details

- Design to utilize maximum of a wafer



Layer	Sensor-A	Sensor-B	Z-Total [mm]	Required [mm]
0	18 mm x 5 chips	18 mm x 5 chips	180	174
1	16 mm x 8 = 128 mm	20 mm x 5 = 100 mm	228	198
2				223
3				247

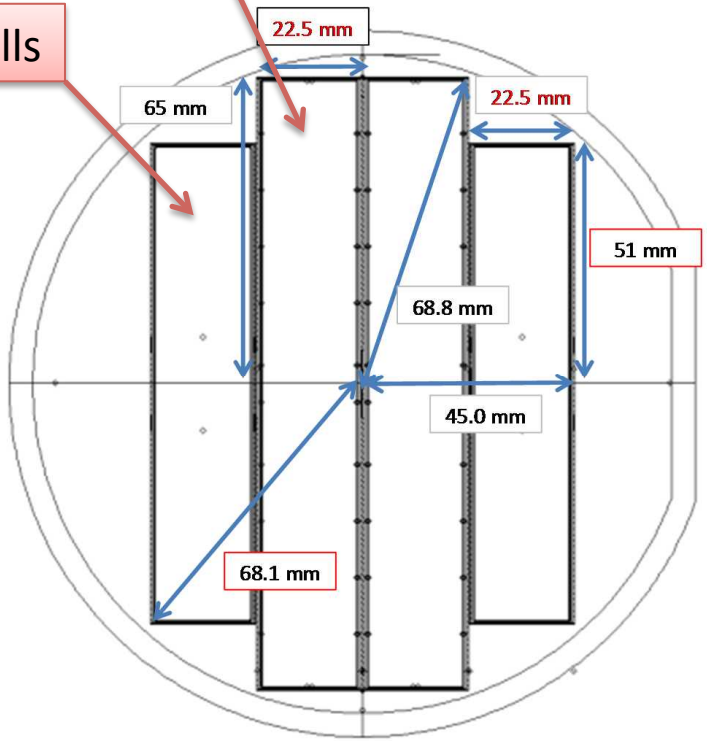
Mostly covers required z, except for the last layer.

Layer-1,2,3 Silicon Sensors

Sensor Layouts in 6 inch Wafer

16mm strip x 8 cells

20mm strip x 5 cells



Maximum Sensor length is 135mm for 22.5mm width sensor

※左図

赤字(幅):記載ミス

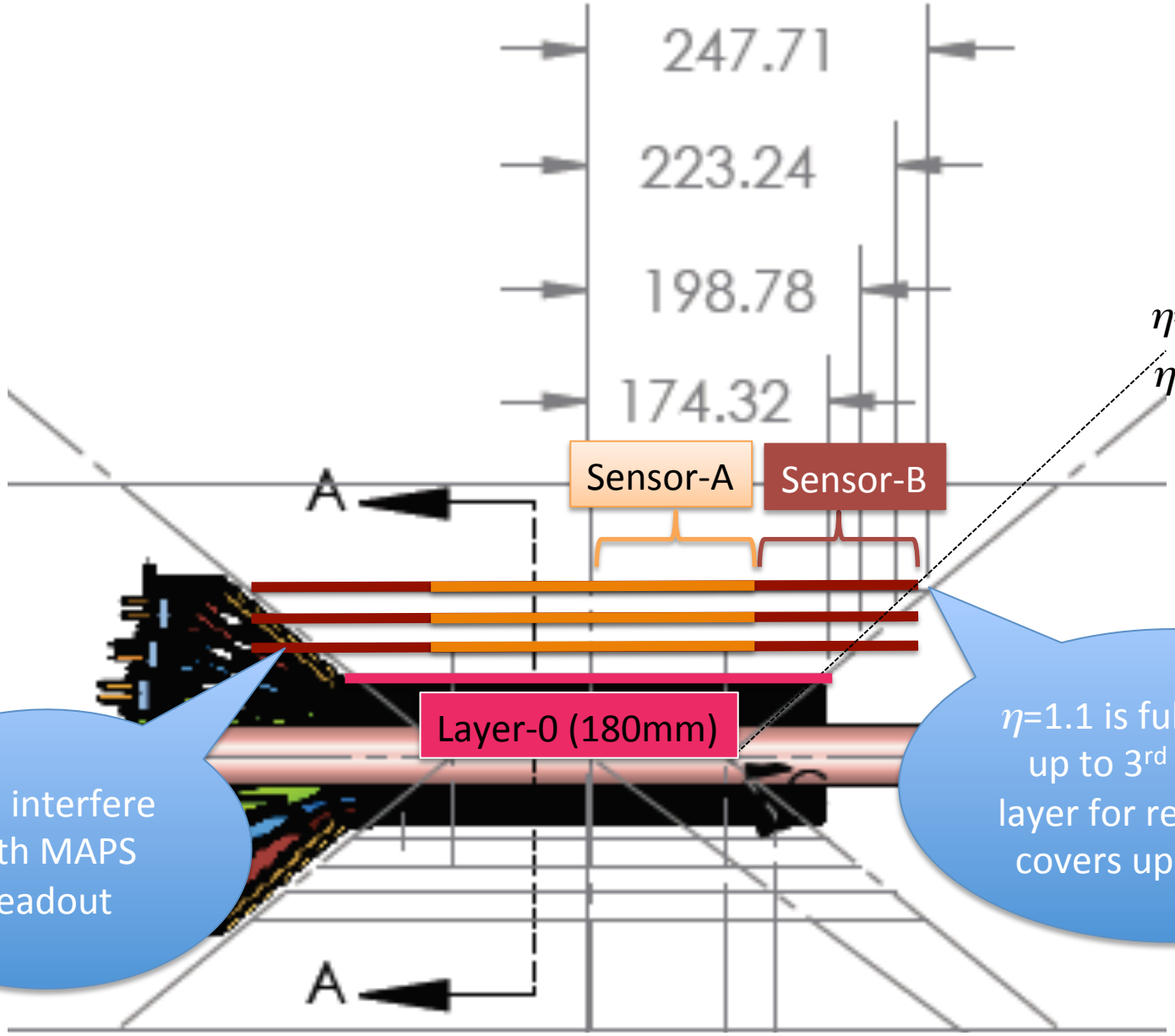
赤枠:修正

Strip length = 20mm
Number of cells = 5

Strip length=16mm x 8 cells = 64mm
Strip length=20mm x 5 cells = 10mm

} x 2 sensors will fit in 1 wafer

Detector Layout



η=1.0 @ z=+10cm

η=1.1 @ z=+10cm

Will interfere with MAPS readout

η=1.1 is fully covered up to 3rd layer. 4th layer for redundancy, covers up to η=1.0.

ROC Ports Configuration

- For one arm

	INTT	Available # of Ports
Layer-0	36	48
Layer-1,2,3	90	144

Number of ports to be used nicely fits within available number of ports

Summary

- Longer INTT design is presented. Extension is done by:
  - 10 FPHX chips/side/SM -> 13 FPHX chip/side/SM
  - Longer strip length than 12mm and two sections (16mm and 20mm)
- **One side readout will introduce double radiation length of INTT. We conclude this is out of option.**
- New design composed by 2 silicon sensors to cover longer-z. Due to constraints from ROC readouts, 10 or 26 chips per port, strip length needs to be longer than original 12mm.
- Layer-0 Covers 180mm with 18mm strips.
- Layer-1,2,3 Covers 228mm with 16mm and 20mm strips.
- Need to coordinate with LANL engineering design of the MAPS and INTT readouts.

BACKUP

Si-Sensor Predicted Dark Current

Sensor Dimension z[mm] x #cell	Thickness 200 μm (per cell)	Thickness 320 μm (per cell)
12 x 10	1600 (160)	400 (40)
16 x 8	1400 (175)	350 (44)
20 x 5	1700 (340)	450 (90)

Silicon Sensor
78μm pitch
128 channel/cell